WHAT IS CLAIMED IS:

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1. A latch circuit which receives a pulse signal and a clock signal as inputs and transmits the pulse signal in synchronization with the clock signal,

the clock signal or the pulse signal having amplitude smaller than amplitude of the pulse signal outputted from the latch circuit.

2. A latch circuit as claimed in claim 1, further comprising a first circuit having a voltage holding function and a second circuit having a level shifting function, the first and second circuits being constructed so as to own some common elements.

3. A latch circuit as claimed in claim 2, wherein the latch circuit is supplied with a power potential, and an element for controlling the voltage holding function or the level shifting function of the input signal is provided between the power potential and the second circuit.

4. A latch circuit as claimed in claim 1, the latch circuit comprising:

a first p-type transistor and a second p-type transistor, having source electrodes connected to the power potential and gate electrodes connected to drain electrodes of the counterparts;

a first n-type transistor having a source electrode connected to the drain electrode of the first p-

type transistor, a drain electrode connected to a ground potential and a gate electrode connected to the drain electrode of the second p-type transistor;

a second n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the drain electrode of the first p-type transistor;

a third n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode that receives the pulse signal as an input;

a fourth n-type transistor having a source electrode connected to the drain electrode of the third n-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the clock signal as an input;

a fifth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode that receives an inverted signal of the pulse signal as an input; and

a sixth n-type transistor having a source electrode connected to the drain electrode of the fifth n-type transistor, a drain electrode connected to the ground

potential and a gate electrode that receives the clock signal as an input,

whereby the pulse signal is outputted from the drain electrode of the second p-type transistor, and the inverted signal of the pulse signal is outputted from the drain electrode of the first p-type transistor.

5. A latch circuit as claimed in claim 1, the latch circuit comprising:

a first p-type transistor and a second p-type transistor, having source electrodes connected to the power potential and gate electrodes connected to drain electrodes of the counterparts;

a first n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode connected to the drain electrode of the second p-type transistor;

a seventh n-type transistor having a source electrode connected to the drain electrode of the first n-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives an inverted signal of the clock signal as an input;

a second n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode connected to the drain electrode of the first p-type transistor;

an eighth n-type transistor having a source electrode connected to the drain electrode of the second n-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the inverted signal of the clock signal as an input;

a third n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode that receives the pulse signal as an input;

a fourth n-type transistor having a source electrode connected to the drain electrode of the third n-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the clock signal as an input;

a fifth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode that receives an inverted signal of the pulse signal as an input; and

a sixth n-type transistor having a source electrode connected to the drain electrode of the fifth n-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the clock signal as an input,

whereby the pulse signal is outputted from the drain electrode of the second p-type transistor, and the

inverted signal of the pulse signal is outputted from the drain electrode of the first p-type transistor.

6. A latch circuit as claimed in claim 1, the latch circuit comprising:

a first p-type transistor and a second p-type transistor, having source electrodes connected to the power potential and gate electrodes connected to drain electrodes of the counterparts;

a first n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode connected to the drain electrode of the second p-type transistor;

a second n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode connected to the drain electrode of the first p-type transistor;

a third n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode that receives the pulse signal as an input;

a fifth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode that receives an inverted signal of the pulse signal as an input; and

a ninth n-type transistor having a source electrode connected to the drain electrodes of the third and fifth n-type transistors, a drain electrode connected to the ground potential and a gate electrode that receives the clock signal as an input; and

a tenth n-type transistor having a source electrode connected to the drain electrodes of the first and second n-type transistors, a drain electrode connected to the ground potential and a gate electrode that receives the inverted signal of the clock signal as an input,

whereby the pulse signal is outputted from the drain electrode of the second p-type transistor, and the inverted signal of the pulse signal is outputted from the drain electrode of the first p-type transistor.

7. A latch circuit as claimed in claim 1, the latch circuit comprising:

a first p-type transistor and a second p-type transistor, having source electrodes connected to the power potential and gate electrodes connected to drain electrodes of the counterparts;

a first n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor, a drain electrode connected to a ground potential and a gate electrode connected to the drain electrode of the second p-type transistor;

a second n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the drain electrode of the first p-type transistor;

a third n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode that receives the pulse signal as an input;

a fifth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode that receives an inverted signal of the pulse signal as an input; and

a ninth n-type transistor having a source electrode connected to the drain electrodes of the third and fifth n-type transistors, a drain electrode connected to the ground potential and a gate electrode that receives the clock signal as an input,

whereby the pulse signal is outputted from the drain electrode of the second p-type transistor, and the inverted signal of the pulse signal is outputted from the drain electrode of the first p-type transistor.

8. A latch circuit as claimed in claim 1, the latch circuit being comprised of first and second logical product and non-disjunction circuits,

the logical product circuit section of the first logical product and non-disjunction circuit receiving the clock signal and the pulse signal as inputs, the non-disjunction circuit section of the first logical product and non-disjunction circuit receiving an output signal of the logical product circuit section and an output signal of the second logical product and non-disjunction circuit as inputs,

the logical product circuit section of the second logical product and non-disjunction circuit receiving the clock signal and the inverted signal of the pulse signal as inputs, and the non-disjunction circuit section of the second logical product and non-disjunction circuit receiving an output signal of the logical product circuit section and an output signal of the first logical product and non-disjunction circuit.

9. A latch circuit as claimed in claim 8, wherein the logical product and non-disjunction circuit comprises:

a first p-type transistor and a second p-type transistor having source electrodes connected to the power potential and gate electrodes connected to the drain electrodes of the counterparts;

a first n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor, a drain electrode connected to the ground

potential and a gate electrode that receives the output signal of the other logical product and non-disjunction circuit as an input;

an eleventh n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode that receives the inverted signal of the clock signal;

a third n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode that receives the pulse signal as an input;

a fourth n-type transistor having a source electrode connected to the drain electrode of the third n-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the clock signal as an input;

a fifth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode that receives the inverted signal of the pulse signal as an input; and

a twelfth n-type transistor having a source electrode connected to the drain electrodes of the eleventh and fifth n-type transistors, a drain electrode connected to the ground potential and a gate electrode that receives

the inverted signal of the output signal of the other logical product and non-disjunction circuit as an input,

whereby the pulse signal is outputted from the drain electrode of the first p-type transistor, and the inverted signal of the pulse signal is outputted from the drain electrode of the second p-type transistor.

10. A latch circuit as claimed in claim 1, the latch circuit comprising:

a first non-conjunction circuit that receives the clock signal and the pulse signal as inputs;

a second non-conjunction circuit that receives the clock signal and the inverted signal of the pulse signal as inputs;

a third non-conjunction circuit that receives an output signal of the first non-conjunction circuit and an output signal of a fourth non-conjunction circuit as inputs; and

the fourth non-conjunction circuit that receives an output signal of the second non-conjunction circuit and an output signal of the third non-conjunction circuit as inputs.

11. A latch circuit as claimed in claim 10, wherein the first and second non-conjunction circuits comprises:

a first p-type transistor and a second p-type transistor, having source electrodes connected to the power

potential and gate electrodes connected to the drain electrodes of the counterparts;

a third n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode that receives the pulse signal as an input;

a fourth n-type transistor having a source electrode connected to the drain electrode of the third n-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the clock signal as an input;

a thirteenth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the inverted signal of the pulse signal as an input; and

a fourteenth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor, a drain electrode connected to the ground potential and a gate electrode that receives the inverted signal of the clock signal as an input,

whereby the output signal of the first non-conjunction circuit is outputted from the drain electrode of the first p-type transistor, and the inverted signal of

the output signal is outputted from the drain electrode of the second p-type transistor.

12. A latch circuit as claimed in claim 1, the latch circuit comprising:

first and second p-type transistors having source electrodes connected to the power potential;

third and fourth p-type transistors having source electrodes connected respectively to the drain electrodes of the first and second p-type transistors, and gate electrodes connected to the clock signal;

third and fifth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, and gate electrodes connected respectively to an input pulse signal and an inverted signal of the input pulse signal;

fourth and sixth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fifth n-type transistors, gate electrodes connected to the clock signal, and drain electrodes connected to the ground potential; and

first and second n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, gate electrodes connected respectively to the drain electrodes of the

fourth and third p-type transistors, and drain electrodes connected to the ground potential,

whereby the output pulse is outputted from the drain electrode of the fourth p-type transistor, and the inverted signal of the output pulse is outputted from the drain electrode of the third p-type transistor.

13. A latch circuit as claimed in claim 1, the latch circuit comprising:

first and second p-type transistors having source electrodes connected to the power potential;

third and fourth p-type transistors having source electrodes connected respectively to the drain electrodes of the first and second p-type transistors, and gate electrodes connected to the clock signal;

third and fifth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, and gate electrodes connected respectively to an input pulse signal and an inverted signal of the input pulse signal;

fourth and sixth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fifth n-type transistors, gate electrodes connected to the clock signal, and drain electrodes connected to the ground potential;

first and second n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, and gate electrodes connected respectively to the drain electrodes of the fourth and third p-type transistors; and

seventh and eighth n-type transistors having source electrodes connected respectively to the drain electrodes of the first and second n-type transistors, gate electrodes connected to the inverted signal of the clock signal, and drain electrodes connected to the ground potential,

whereby the output pulse is outputted from the drain electrode of the fourth p-type transistor, and the inverted signal of the output pulse is outputted from the drain electrode of the third p-type transistor.

14. A latch circuit as claimed in claim 1, the latch circuit comprising:

first and second p-type transistors having source electrodes connected to the power potential;

third and fourth p-type transistors having source electrodes connected respectively to the drain electrodes of the first and second p-type transistors, and gate electrodes connected to the clock signal;

fifth and sixth p-type transistors having source electrodes connected respectively to the drain electrodes

of the first and second p-type transistors, gate electrodes connected respectively to an input pulse signal and an inverted signal of the input pulse signal, and drain electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors;

third and fifth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, and gate electrodes connected respectively to the input pulse signal and the inverted signal of the input pulse signal;

fourth and sixth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fifth n-type transistors, gate electrodes connected to the clock signal, and drain electrodes connected to the ground potential; and

first and second n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, gate electrodes connected respectively to the drain electrodes of the fourth and third p-type transistors, and drain electrodes connected to the ground potential;

whereby the output pulse is outputted from the drain electrode of the fourth p-type transistor, and the inverted signal of the output pulse is outputted from the drain electrode of the third p-type transistor.

15. A latch circuit as claimed in claim 1, the latch circuit comprising:

first and second p-type transistors having source electrodes connected to the power potential;

third and fourth p-type transistors having source electrodes connected respectively to the drain electrodes of the first and second p-type transistors, and gate electrodes connected to the clock signal;

fifth and sixth p-type transistors having source electrodes connected respectively to the drain electrodes of the first and second p-type transistors, gate electrodes connected respectively to an input pulse signal and an inverted signal of the input pulse signal, and drain electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors;

third and fifth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, and gate electrodes connected respectively to the input pulse signal and the inverted signal of the input pulse signal;

fourth and sixth n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fifth n-type transistors, gate electrodes connected to the clock signal, and drain electrodes connected to the ground potential;

first and second n-type transistors having source electrodes connected respectively to the drain electrodes of the third and fourth p-type transistors, and gate electrodes connected respectively to the drain electrodes of the fourth and third p-type transistors; and

seventh and eighth n-type transistors having source electrodes connected respectively to the drain electrodes of the first and second n-type transistors, gate electrodes connected to an inverted signal of the clock signal, and drain electrodes connected to the ground potential,

whereby the output pulse is outputted from the drain electrode of the fourth p-type transistor, and the inverted signal of the output pulse is outputted from the drain electrode of the third p-type transistor.

16. A latch circuit as claimed in claim 9, wherein the first, second, third and fifth n-type transistors have a dual-gate structure, and the fourth, sixth, seventh and eighth n-type transistors have a single-gate structure.

17. A latch circuit as claimed in claim 9, wherein the first, second, third and fifth n-type transistors have a channel length longer than the channel length of the fourth, sixth, seventh and eighth n-type transistors.

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18. A shift register circuit having a plurality of latch circuits for transmitting a pulse signal in synchronization with a clock signal,

the latch circuits each internally having a clock signal input control section for executing control to input and stop the supplied clock signal, and

the clock signal having amplitude smaller than the amplitude of the pulse signal.

19. A shift register circuit as claimed in claim 18, wherein

the clock signal inputted to the latch circuits is only either one of a clock signal of a specified cycle and an antiphase signal of the clock signal.

20. A shift register circuit as claimed in claim 18 wherein an output signal of each of the latch circuits is inputted to the latch circuit of the succeeding stage via a first transfer gate and inputted to the latch circuit of the preceding stage via a second transfer gate, and a scanning direction is controlled by selectively making conductive the first or second transfer gate by means of an external signal.

21. A shift register circuit as claimed in claim 18, wherein an output signal of each of the latch circuits is inputted to the latch circuit of the succeeding stage via a buffer circuit.

22. A shift register circuit as claimed in claim 18, wherein

the clock signal input control section is comprised of a first clock signal input control section and a second clock signal input control section, and

the latch circuit comprises:

a first p-type transistor and a second p-type transistor having source electrodes connected to a power potential and gate electrodes connected to drain electrodes of the counterparts;

a first n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor, a drain electrode connected to a ground potential and a gate electrode connected to the drain electrode of the second p-type transistor;

a second n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the drain electrode of the first p-type transistor;

a third n-type transistor having a source electrode connected to the drain electrode of the first p-type transistor and a gate electrode connected to a pulse signal input node;

a fourth n-type transistor having a source electrode connected to the drain electrode of the third n-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the first clock signal input control section;

a fifth n-type transistor having a source electrode connected to the drain electrode of the second p-type transistor and a gate electrode connected to an inverted pulse signal input node; and

a sixth n-type transistor having a source electrode connected to the drain electrode of the fifth n-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the second clock signal input control section,

whereby the drain electrode of the second p-type transistor is made to serve as a pulse signal output node and the drain electrode of the first p-type transistor is made to serve as an inverted pulse signal output node.

23. A shift register circuit as claimed in claim 22, wherein

the latch circuit comprises:

a first inverter having an input terminal connected to the inverted pulse signal output node; and

a second inverter having an input terminal connected to the pulse signal output node,

whereby the output terminal of the first inverter is made to serve as a new pulse signal output node and the output terminal of the second inverter is made to serve as a new inverted pulse signal output node.

24. A shift register circuit as claimed in claim 22, wherein

the first clock signal input control section is comprised of a switching means for electrically disconnecting the gate electrode of the fourth n-type transistor from the clock signal input node when the latch circuit becomes inactive and a potential fixing means for fixing the potential of the gate electrode of the fourth n-type transistor that is electrically disconnected from the clock signal input node at a specified potential, and

the second clock signal input control section is comprised of a switching means for electrically disconnecting the gate electrode of the sixth n-type transistor from the clock signal input node when the latch circuit becomes inactive and a potential fixing means for fixing the potential of the gate electrode of the sixth n-type transistor that is electrically disconnected from the clock signal input node at a specified potential.

25. A shift register circuit as claimed in claim 24 wherein

the switching means of the first clock signal input control section is comprised of a fifteenth n-type transistor having a source electrode connected to the clock signal input node, a drain electrode connected to the gate electrode of the fourth n-type transistor and a gate electrode connected to the pulse signal input node, and

the switching means of the second clock signal input control section is comprised of a sixteenth n-type transistor having a source electrode connected to the clock signal input node, a drain electrode connected to the gate electrode of the sixth n-type transistor and a gate electrode connected to the pulse signal output node.

26. A shift register circuit as claimed in claim 24, wherein

the potential fixing means of the first clock signal input control section is comprised of a seventeenth n-type transistor having a source electrode connected to the gate electrode of the fourth n-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the power potential, and

the potential fixing means of the second clock signal input control section is comprised of an eighteenth n-type transistor having a source electrode connected to the gate electrode of the sixth n-type transistor, a drain electrode

electrode connected to the ground potential and a gate electrode connected to the power potential.

27. A shift register circuit as claimed in claim 24, wherein

the potential fixing means of the first clock signal input control section is comprised of a nineteenth n-type transistor having a source electrode connected to the gate electrode of the fourth n-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to its own source electrode, and

the potential fixing means of the second clock signal input control section is comprised of a twentieth n-type transistor having a source electrode connected to the gate electrode of the sixth n-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to its own source electrode.

28. A shift register circuit as claimed in claim 24, wherein

the potential fixing means of the first clock signal input control section is comprised of a first resistor provided between the gate electrode of the fourth n-type transistor and the ground potential, and

the potential fixing means of the second clock signal input control section is comprised of a second

resistor provided between the gate electrode of the sixth n-type transistor and the ground potential.

29. A shift register circuit as claimed in claim 25, wherein

the potential fixing means of the first clock signal input control section is comprised of a twenty-first n-type transistor having a source electrode connected to the gate electrode of the fourth n-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the inverted pulse signal input node, and

the potential fixing means of the second clock signal input control section is comprised of a twenty-second n-type transistor having a source electrode connected to the gate electrode of the sixth n-type transistor, a drain electrode connected to the ground potential and a gate electrode connected to the inverted pulse signal output node.

30. An active matrix type image display device comprising: a plurality of data signal lines arranged in a direction of column; a plurality of scanning signal lines arranged in a direction of row; a plurality of pixels that are arranged in a matrix form while being placed in positions surrounded by the data signal lines and the scanning signal lines; a data signal line drive circuit for

supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines,

at least one of the data signal line drive circuit and the scanning signal line drive circuit being comprised of the shift register circuit claimed in any one of claims 18 through 29.

31. An active matrix type image display device comprising: a plurality of data signal lines arranged in a direction of column; a plurality of scanning signal lines arranged in a direction of row; a plurality of pixels that are arranged in a matrix form while being placed in positions surrounded by the data signal lines and the scanning signal lines; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines,

one of the signal line drive circuits is comprised of the shift register circuit claimed in claim 22 and

constructed so as to generate a drive signal for driving the corresponding signal line by means of an output signal that has a narrower pulse width out of the two output signals of the pulse signal and the inverted pulse

signal from each latch circuit constituting the shift register circuit.

32. An image display device as claimed in claim 30, comprising:

a level shifter circuit that amplifies the amplitude of a start signal having the same amplitude as that of the clock signal and supplies the resulting signal as the pulse signal to the latch circuit of the first stage in the shift register circuit of the one signal line drive circuit.

33. An image display device as claimed in claim 30, comprising:

a level shifter circuit that amplifies the amplitude of a control signal having the same amplitude as that of the clock signal and supplies the resulting signal to the one signal line drive circuit.

34. An image display device as claimed in claim 30, wherein

at least one of the signal line drive circuit is formed on a substrate identical to that of the pixels.

35. An image display device as claimed in claim 34, wherein

an active element that constitutes at least one of the signal line drive circuit and the pixels is a polysilicon thin-film transistor.

36. An image display device as claimed in claim 35, wherein

the polysilicon thin-film transistor is formed on a glass substrate through a process at a temperature of not higher than 600°C.

37. A CMOS logical circuit consisting of Complementary Metal-Oxide Semiconductors which performs a logical operation based on a plurality of input signals,

an amplitude of at least one of the input signals is smaller than a drive voltage of the CMOS logical circuit.

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38. A logical circuit as claimed in claim 37 comprising two electric current paths each of which has a circuit consisting of at least one n-type transistor and a circuit consisting of at least one p-type transistor, wherein

as concerns the circuit having one of the n-type transistor and the p-type transistor,

the one electric current path is provided with a circuit having the same construction as that of a circuit having an n-type transistor of a CMOS logical circuit outputting a logical operation result similar to that of the logical circuit, and

the other electric current path is provided with a circuit having the same construction as that of a circuit

having a p-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit, and

as concerns the circuit having the transistor of the other channel type,

a gate electrode of the transistor provided on the one electric current path and that of the transistor provided on the other electric current path are connected to drain electrodes of the counterparts.

39. A logical circuit as claimed in claim 37 comprising two electric current paths each of which has a circuit consisting of at least one n-type transistor and a circuit consisting of at least one p-type transistor, wherein

as concerns the circuit having one of the n-type transistor and the p-type transistor,

the one electric current path is provided with a circuit having the same construction as that of a circuit having an n-type transistor of a CMOS logical circuit outputting a logical operation result similar to that of the logical circuit, and

the other electric current path is provided with a circuit having the same construction as that of a circuit having a p-type transistor of the CMOS logical circuit

outputting the logical operation result similar to that of the logical circuit, and

as concerns the circuit having the transistor of the other channel type,

each of the two electric current paths is provided with a transistor to which at least one of the input signals is inputted to a gate electrode and a transistor at a power source side of each thereof such that a gate electrode of the transistor provided on the one electric current path is connected to an output portion of the other electric current path, and a gate electrode of the transistor provided on the other electric current path is connected to an output portion of the one electric current path.

40. A logical circuit as claimed in claim 37 comprising two electric current paths each of which has a circuit consisting of at least one n-type transistor and a circuit consisting of at least one p-type transistor, wherein

as concerns the circuit having one of the n-type transistor and the p-type transistor of the logical circuit,

the one electric current path is provided with a circuit having the same construction as that of a circuit having an n-type transistor of a CMOS logical circuit

outputting a logical operation result similar to that of the logical circuit, and

the other electric current path is provided with a circuit having the same construction as that of a circuit having a p-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit, and

as concerns the circuit having the transistor of the other channel type,

the one electric current path is provided with the circuit having the same construction as that of the circuit having the p-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit,

the other electric current path is provided with the circuit having the same construction as that of the circuit having the n-type transistor of the CMOS logical circuit outputting the logical operation result similar to that of the logical circuit,

each of the two electric current paths is provided with a transistor at a power source side thereof such that a gate electrode of the transistor provided on the one electric current path is connected to an output portion of the other electric current path, and a gate electrode of the transistor provided on the other electric

current path is connected to an output portion of the one electric current path.

41. A logical circuit as claimed in claim 39, wherein in the n-type circuit or the p-type circuit, a signal having a smaller amplitude than a plurality of the signals is inputted to one transistor positioned farther from the output portion than the other transistor that is connected in series with the one transistor.

42. A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to drain electrodes of the counterparts and connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a drain electrode connected to a source electrode of the third transistor, and a source electrode connected to a second supply potential;

a fifth transistor having a gate electrode connected to a third input terminal, a drain electrode

connected to the first output terminal, and a source electrode connected to the second supply potential; and

a sixth transistor having a gate electrode connected to a fourth input terminal, a drain electrode connected to the first output terminal, and a source electrode connected to the second supply potential; wherein

signals to be inputted to the first and third input terminals are inverse to each other in phase, and signals to be inputted to the second and fourth input terminals are inverse to each other in phase, and

the first and second transistors are of a channel type different from that of the other transistors.

43. A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to drain electrodes of the counterparts and connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a drain electrode

connected to a source electrode of the third transistor, and a source electrode connected to a second supply potential;

a fifth transistor having a gate electrode connected to a third input terminal, a drain electrode connected to the second output terminal, and a source electrode connected to the second supply potential;

a sixth transistor having a gate electrode connected to a fourth input terminal and a source electrode connected to the second supply potential;

a seventh transistor having a gate electrode connected to a fifth input terminal and a source electrode connected to the second supply potential; and

an eighth transistor having a gate electrode connected to a sixth input terminal, a drain electrode connected to the first output terminal, and a source electrode connected to the drain electrode of the sixth transistor and that of the seventh transistor,

wherein

signals to be inputted to the first and fourth input terminals are inverse to each other in phase, signals to be inputted to the second and fifth input terminals are inverse to each other in phase, and signals to be inputted to the third and sixth input terminals are inverse to each other in phase, and

the first and second transistors are of a channel type different from that of the other transistors.

44. A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to drain electrodes of the counterparts and connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a drain electrode connected to a source electrode of the third transistor, and a source electrode connected to a second supply potential;

a fifth transistor having a gate electrode connected to a third input terminal, a drain electrode connected to the second output terminal, and a source electrode connected to the second supply potential; and

a sixth transistor having a gate electrode connected to a fourth input terminal and a drain electrode connected to the first output terminal;

a seventh transistor having a gate electrode connected to a fifth input terminal and a drain electrode connected to the first output terminal; and

an eighth transistor having a gate electrode connected to a sixth input terminal, a drain electrode connected to a source electrode of the sixth transistor and that of the seventh transistor, and a source electrode connected to the second supply potential,

wherein

signals to be inputted to the first and fifth input terminals are inverse to each other in phase, signals to be inputted to the second and fourth input terminals are inverse to each other in phase, and signals to be inputted to the third and sixth input terminals are inverse to each other in phase, and

the first and second transistors are of a channel type different from that of the other transistors.

45. A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal, a source electrode

connected to a drain electrode of the first transistor, and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to the drain electrode of a second transistor, and a drain electrode connected to the first output terminal;

a fifth transistor having a gate electrode connected to a third input terminal and a drain electrode connected to the second output terminal;

a sixth transistor having a gate electrode connected to the first input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the fifth transistor;

a seventh transistor having a gate electrode connected to a fourth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal; and

an eighth transistor having a gate electrode connected to the second input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal,

wherein

signals to be inputted to the first and second input terminals are inverse to each other in phase, signals to be inputted to the third and fourth input terminals are inverse to each other in phase, and

the first through fourth transistors are of a channel type different from that of the other transistors.

46. A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal, a source electrode connected to a drain electrode of the first transistor, and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to the drain electrode of a first transistor, and a drain electrode connected to the second output terminal;

a fifth transistor having a gate electrode connected to a third input terminal, and a source electrode connected to a drain electrode of the second transistor;

a sixth transistor having a gate electrode connected to a fourth input terminal, a source electrode

connected to a drain electrode of the fifth transistor, and a drain electrode connected to the first output terminal;

a seventh transistor having a gate electrode connected to a fifth input terminal and a drain electrode connected to the second output terminal;

an eighth transistor having a gate electrode connected to the second input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the seventh transistor,

a ninth transistor having a gate electrode connected to a sixth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal, and

a 10th transistor having a gate electrode connected to the fourth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the first output terminal,

wherein

signals to be inputted to the first and third input terminals are inverse to each other in phase, and signals to be inputted to the second and fourth input terminals are inverse to each other in phase, and

the first through sixth transistors are of a channel type different from that of the other transistors.

47. A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal, a source electrode connected to a drain electrode of the first transistor, and a drain electrode connected to the second output terminal;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to a drain electrode of the second transistor, and a drain electrode connected to the first output terminal;

a fifth transistor having a gate electrode connected to a third input terminal, and a drain electrode connected to the second output terminal;

a sixth transistor having a gate electrode connected to the first input terminal, a source electrode connected to a second supply potential, and a drain electrode connected to a source electrode of the fifth transistor;

a seventh transistor having a gate electrode connected to a fourth input terminal, a source electrode

connected to the second supply potential, and a drain electrode connected to the second output terminal;

an eighth transistor having a gate electrode connected to a fifth input terminal, and a drain electrode connected to the first output terminal,

a ninth transistor having a gate electrode connected to the second input terminal, and a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the eighth transistor, and

a 10th transistor having a gate electrode connected to a sixth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the eighth transistor,

wherein

signals to be inputted to the first and second input terminals are inverse to each other in phase, signals to be inputted to the third and sixth input terminals are inverse to each other in phase, and signals to be inputted to the fourth and fifth input terminals are inverse to each other in phase, and

the first through fourth transistors are of a channel type different from that of the other transistors.

48. A logical circuit as claimed in claim 37 comprising:

first and second transistors having source electrodes connected to a first electrode potential and gate electrodes connected to a first output terminal and a second output terminal, respectively,

a third transistor having a gate electrode connected to a first input terminal and a source electrode connected to a drain electrode of the first transistor;

a fourth transistor having a gate electrode connected to a second input terminal, a source electrode connected to a drain electrode of the third transistor, and a drain electrode connected to the second output terminal;

a fifth transistor having a gate electrode connected to a third input terminal, a source electrode connected to a drain electrode of the third transistor, and a drain electrode connected to the second output terminal;

a sixth transistor having a gate electrode connected to a fourth input terminal, a source electrode connected to a drain electrode of the second transistor, and a drain electrode connected to the first output terminal;

a seventh transistor having a gate electrode connected to a fifth input terminal and a source electrode connected to the drain electrode of the second transistor;

an eighth transistor having a gate electrode connected to a sixth input terminal, a source electrode connected to a drain electrode of the seventh transistor, and a drain electrode connected to the first output terminal;

a ninth transistor having a gate electrode connected to a seventh input terminal and a drain electrode connected to the second output terminal;

a 10th transistor having a gate electrode connected to an eighth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the ninth transistor,

an 11th transistor having a gate electrode connected to a ninth input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the second output terminal,

a 12th transistor having a gate electrode connected to a 10th input terminal and a drain electrode connected to the first output terminal;

a 13th transistor having a gate electrode connected to an 11th input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to a source electrode of the 12th transistor, and

a 14th transistor having a gate electrode connected to a 12th input terminal, a source electrode connected to the second supply potential, and a drain electrode connected to the source electrode of the 12th transistor,

wherein

signals to be inputted to the first and fourth input terminals are inverse to each other in phase, signals to be inputted to the second and sixth input terminals are inverse to each other in phase, and signals to be inputted to the third and fifth input terminals are inverse to each other in phase, and

the first through eighth transistors are of a channel type different from that of the other transistors.

49. A logical circuit as claimed in claim 37, wherein at least one of the input signals is inputted through a transfer transistor for controlling an input of the signals.

50. A logical circuit as claimed in claim 49, wherein a malfunction prevention transistor is connectedly provided between a specified supply potential and a gate electrode of a transistor to which a signal controlled by the transfer transistor is inputted, and

the gate electrode of the malfunction prevention transistor is connected to a supply potential different from the special supply potential.

51. A logical circuit as claimed in claim 49, wherein a malfunction prevention transistor is connectedly provided between a specified supply potential and a gate electrode of a transistor to which a signal controlled by a transfer transistor is inputted, and

a signal having a phase inverse to that of a signal to be inputted to the transfer transistor is inputted to a gate electrode of the malfunction prevention transistor.

52. A logical circuit as claimed in claim 49, wherein any one of the input signals is inputted to a gate electrode of a transfer transistor.

53. An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the data signal line drive circuit and/or the scanning signal line drive circuit has the logical circuit as claimed in claim 37.

54. An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the data signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.

55. An image display device cmprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal

to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.

56. An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as at least one part of a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and one of a plurality of control signals inputted from outside as input signals

and outputting signals simultaneously to a plurality of shift register circuits having a different combination.

57. An image display device as claimed in claim 54, wherein in the logical circuit constituting the data signal line drive circuit and the scanning signal line drive circuit, an output signal of the shift register circuit is inputted to a gate electrode of the transfer transistor.

58. An image display device as claimed in claim 53, wherein the data signal line drive circuit and/or the scanning signal line drive circuit is formed on a substrate identical to that of the pixels.

59. An image display device as claimed in claim 58, wherein an active element that constitutes at least one of the signal line drive circuits and the pixels is a polysilicon thin-film transistor.

60. An image display device as claimed in claim 59, wherein the active element is formed through a process at a temperature of not higher than 600℃.

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